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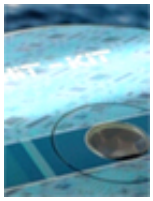
Austriamicrosystems – Enhanced high-voltage CMOS design kit for Mentor Graphics IC Flow



An update of the analog/mixed-signal high-performance technology design kit (HIT-Kit) based on Mentor Graphics IC Flow 2005.1 has been announced by Austriamicrosystems for its advanced 0.35µm high-voltage CMOS technology. The new design environment includes the latest enhancements of the company's 0.35µm high-voltageCMOS process technology H35.

The HIT-Kit v3.71 contains improved high-voltage devices, physical verification rule sets for Calibre DRC/LVS, device model files for Calibre xRC as well as the digital and analog periphery libraries with improved ESD protection. A set of very accurate circuit simulation models which now consider parasitic bipolars on high-voltage devices, layout generators and special layout verification utilities like leakage check, complete the easy to use HIT-Kit that enables foundry users to create robust analog/high-voltage product designs.

"Using our new high-voltage CMOS HIT-Kit with its updated devices and libraries enables foundry customers to complete their high-voltage product designs in Mentor's state-of-the-art design environment", said Thomas Riener, marketing director, Austriamicrosystems' Full Service Foundry business unit. "In combination with the performance improvements we achieved with our advanced high-voltage CMOS technology we offer a competitive solution enabling our customers to create first time right designs and reduce time-to-market."

The new Mentor HIT-Kit v3.71 contains a complete set of fully silicon-qualified standard cells, periphery cells and general-purpose analog cells such as comparators, operational amplifiers, low power A/D and D/A converters necessary to rapidly get designs off the ground using Mentor Graphics new IC Flow environment based on ICstudio. Custom analog and high voltage devices, physical verification rule sets for Calibre DRC/LVS and for Calibre xRC parasitic layout extraction, as well as high=performance characterized circuit simulation models enable rapid design starts of complex high performance mixed-signal ICs.

All I/O structures within the design kit are silicon-validated and meet the military ESD and JEDEC latch-up standards with I/O pads designed to surpass 4kV HBM and 250mA latch-up immunity. In C35 technology the total I/O libraries consist of more than 1800 cells supporting 3.3V and 3.3V/5V designs. The specialty high-voltage CMOS process H35 with its floating libraries also includes more than 2400 core and periphery cells, says the company.

Notes